Notice of Allowability	Application No.	Applicant(s)	
	10/707,905	COOLBAUGH ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *1-08-2007 reply*.

2. ☒ The allowed claim(s) is/are *16 and 18-29*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *3/28/2007* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

SHOUXIANG HU
PRIMARY EXAMINER

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Andrew M. Calderon (RN: 38,093) on March 23, 2007.

The application has been amended as follows:

IN THE CLAIMS

16. (Currently amended) A method of fabricating a varactor, comprising:

providing a semiconductor substrate;

doping a lower region of the semiconductor substrate with a first dopant at a first energy level;

doping a middle region of the semiconductor substrate with a second dopant at a second energy level lower than the first energy level, so as to form a hyper-abrupt junction in the middle region; and

doping an upper region of the semiconductor substrate with a third dopant at a third energy level lower than the second energy level, so as to form an anode in the upper region,

wherein the lower region includes a collector region and a cathode of the varactor, and the cathode is extended to a top surface of the semiconductor substrate through a reach-through implant region.

17. (Cancelled).

18. (Previously Presented) The method of claim 16, further comprising selecting the first dopant from a first N-type dopant, selecting the second dopant from a second N-type dopant, and selecting the third dopant from a P-type dopant.

19. (Currently Presented) The method of claim 16, ~~further comprising doping~~ wherein a bottom layer of the lower region ~~of~~ has a higher concentration of the first dopant than an upper layer of the lower region.

20. (Currently Amended) The method of claim 19, ~~further comprising forming a~~ wherein the collector of the varactor is formed in the upper layer of the lower region of the semiconductor substrate.

21. (Previously Presented) The method of claim 16, further comprising forming at least one isolation region adjacent to the lower, middle, and upper regions of the semiconductor substrate.

22. (Currently Amended) The method of claim 16, ~~further comprising forming at least one~~ wherein the reach-through implant region is in electrical communication with the lower region of the semiconductor substrate.

23. (Currently Amended) The method of claim 16, further comprising forming a silicide layer on ~~a~~ the top of the semiconductor substrate above the upper region.

24. (Currently Amended) A method of fabricating a varactor, comprising:

doping a lower region of a substrate layer with a first dopant having a dopant profile such that atoms having a first energy ("A") penetrate to a first depth ("A'") in the substrate layer forming a cathode and atoms having a second energy ("B") penetrate to a second depth ("B'") in the substrate layer forming a collector region above the cathode, wherein A>B and A'>B';

doping a middle region of the substrate layer with a second dopant, so as to form a hyper-abrupt junction in the middle region, the middle region being tailored for an implant profile that forms an anode, the second dopant overlapping the collector region; and

doping an upper region of the substrate layer with a source/drain type implant to form the anode,

wherein the doping of the middle region has approximately less energy than the doping of the lower region and the doping of the upper region has approximately less energy than the doping of the middle region, and

wherein the cathode is extended to a top surface of the semiconductor substrate through a reach-through implant region.

25. (Currently Amended) The method of claim 24, wherein the ~~forming of the~~ collector region and the cathode are formed in a single doping step via energy distribution of a single dopant type.

26. (Previously Presented) The method of claim 24, wherein an active portion of the varactor is formed in a column from the substrate layer which is a semiconductor material.

27. (Previously Presented) The method of claim 16, wherein the second dopant is deposited at a shallower depth than the first dopant and the third dopant is deposited at a shallower depth than the second.

28. (Currently Amended) The method of claim 16, wherein only three doping steps are utilized to form the ~~varactor with a~~ cathode, ~~a~~ the collector, ~~an HA~~ the hyper-abrupt junction, and ~~an~~ the anode of the varactor.

29. (Currently Amended) A method of fabricating a varactor, comprising:

forming a semiconductor substrate;

doping a lower region of the semiconductor substrate with a first dopant at a first energy level;

doping a middle region of the semiconductor substrate with a second dopant at a second energy level lower than the first energy level, so as to form a hyper-abrupt junction in the middle region; and

doping an upper region of the semiconductor substrate with a third dopant at a third energy level lower than the second energy level, so as to form an anode,

wherein the ~~semiconductor substrate~~ lower region includes a collector region and a cathode that are formed in a single doping step via energy distribution of a single dopant type; and

wherein the cathode is extended to a top surface of the semiconductor substrate through a reach-through implant region.

Allowable Subject Matter

Claims 16 and 18-29 are allowed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References A, B and N are cited as being related to the forming of a diode structure though implanting.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Friday, 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SH
March 29, 2007

SHOUXIANG HU
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